

Efficient power electronics enabled by 3.3kV Silicon Carbide Switches

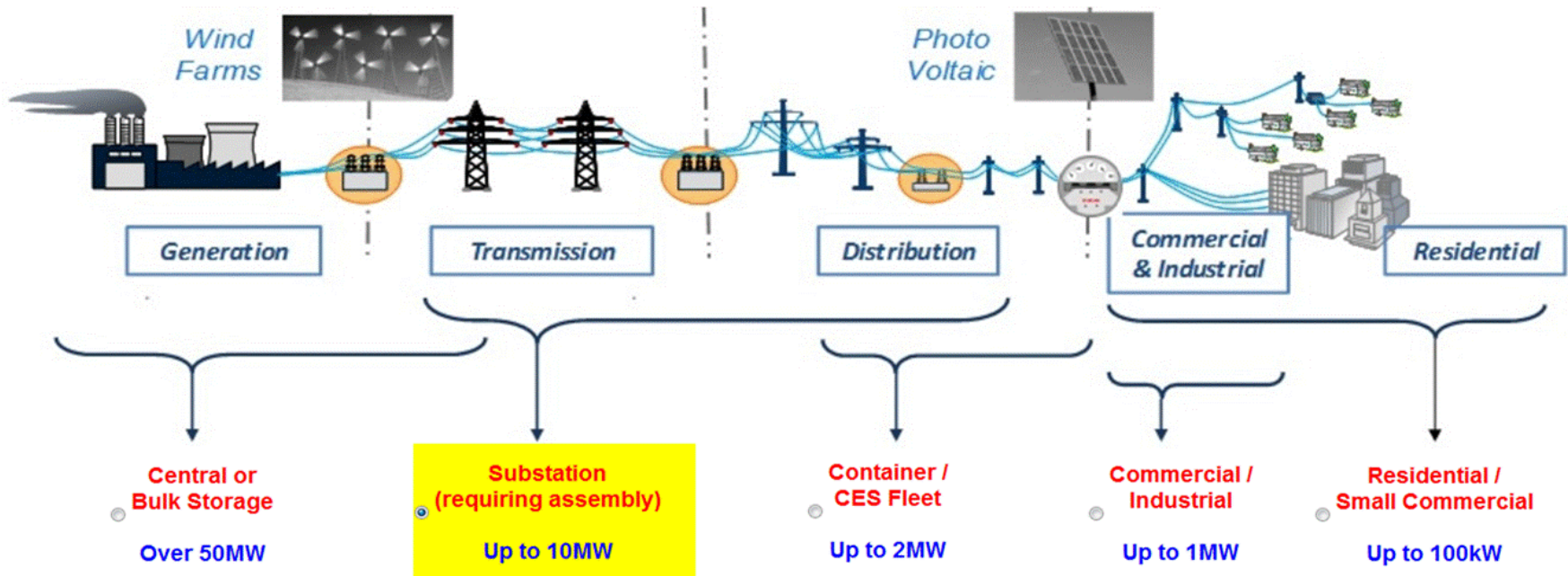
GeneSiC Semiconductor Inc.
NC State University (S. Bhattacharya)
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GeneSiC
SEMICONDUCTOR

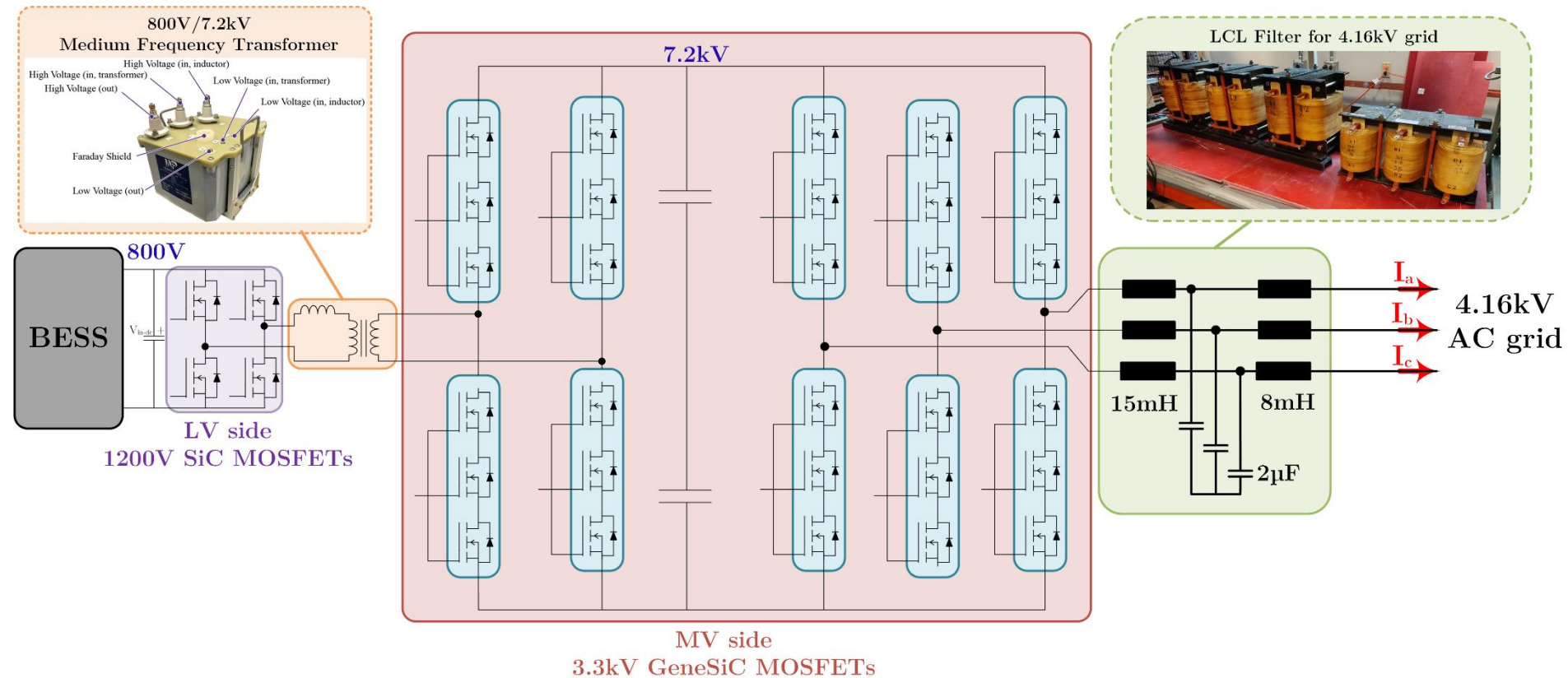
Energy Storage Opportunities at Medium Voltages (4.16 kV-34 kV) Distribution Grid

Possible Locations for Grid-Connected Energy Storage



- Many energy storage opportunities require power electronics that can enable conversion efficiencies needed for making energy storage viable
- Silicon Carbide high voltage devices will play a pivotal role

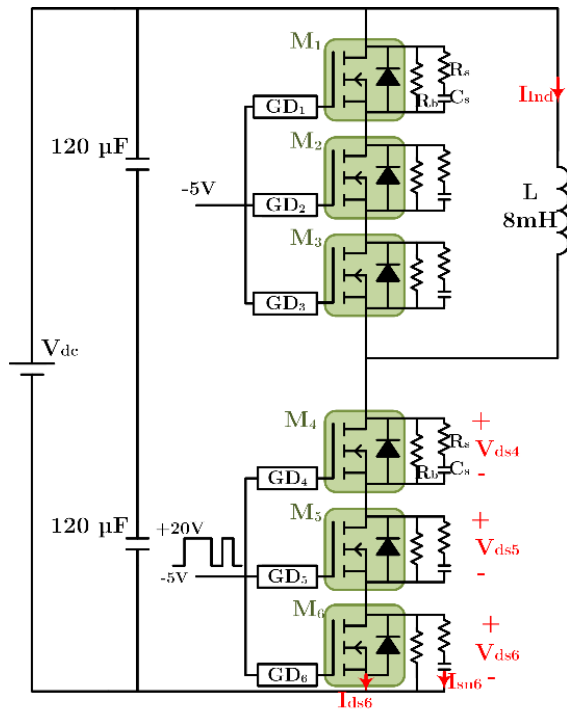
Direct Grid Connection of BESS Enabled by 3.3kV Silicon Carbide MOSFETs



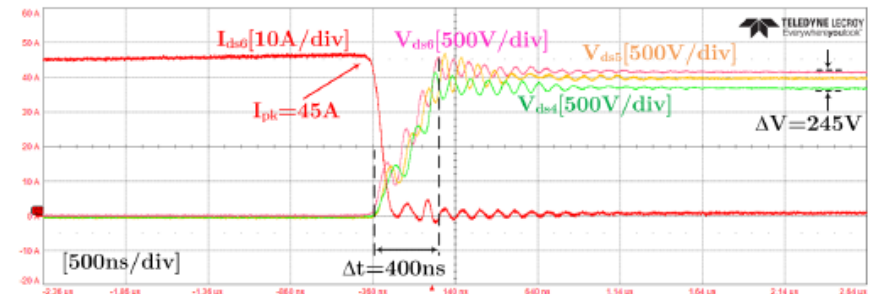
Series connected 3.3kV SiC MOSFET based converter system interfacing a BESS directly to MV grid without 60Hz transformer

Voltage Balancing of Series connected 3.3kV SiC MOSFETs – enabling MV grid interface

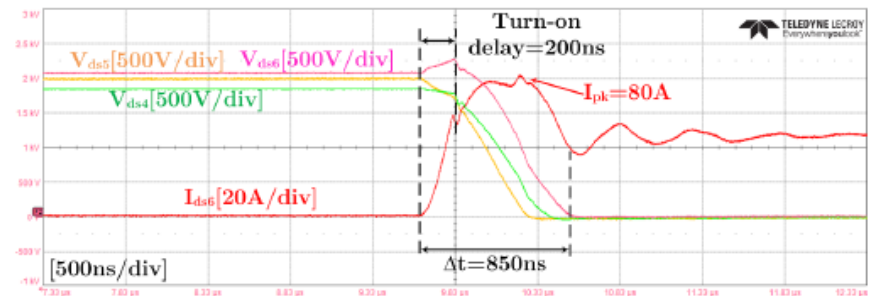
- Static and dynamic voltage balancing among the three series 3.3kV SiC MOSFETs in the series string has been experimentally verified



Double pulse test (DPT) circuit used to characterize series connected 3.3kV SiC MOSFET based switching cell



(a)

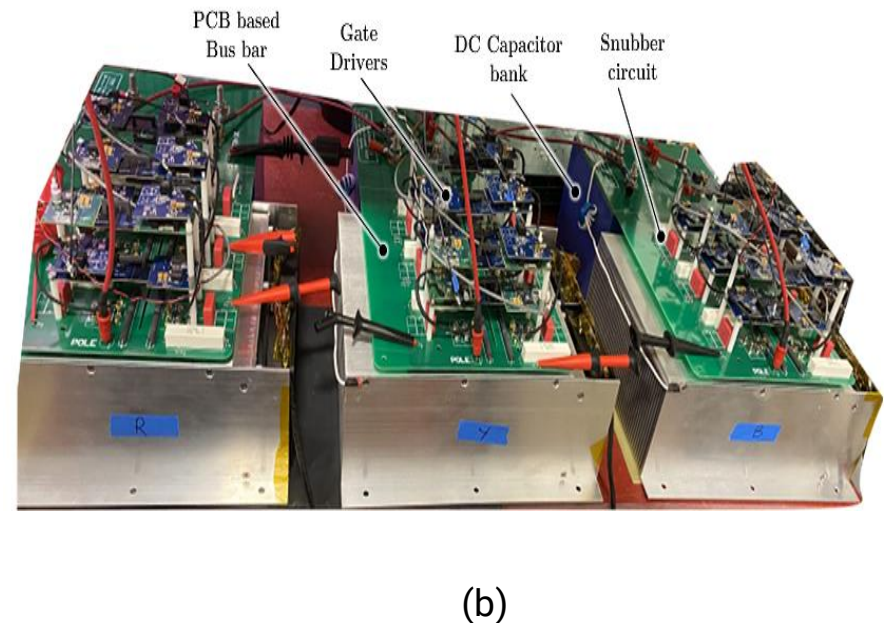
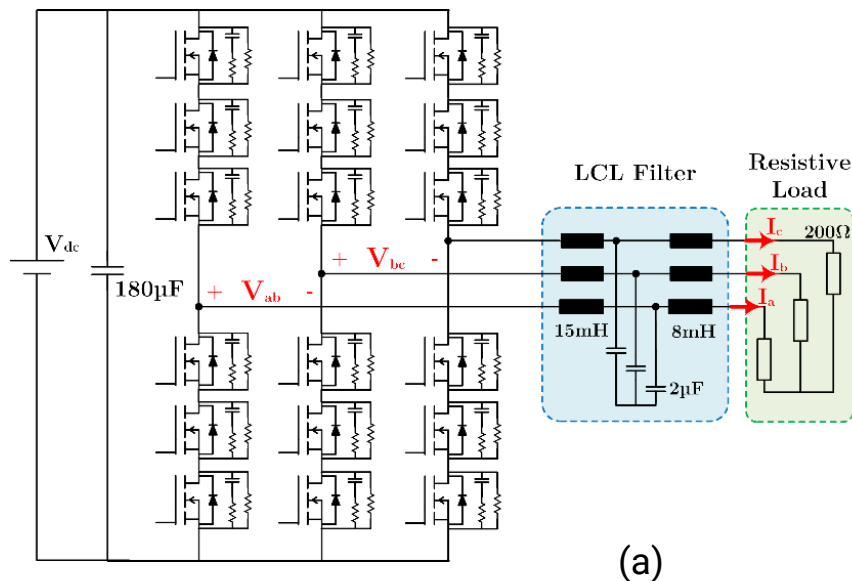


(b)

DPT result of three series-connected 3.3kV 40mΩ SiC MOSFETs at 6kV dc bus and 45A load current
(a) Turn-off transition (b) Turn-on transition ($T_j = 25^\circ\text{C}$)

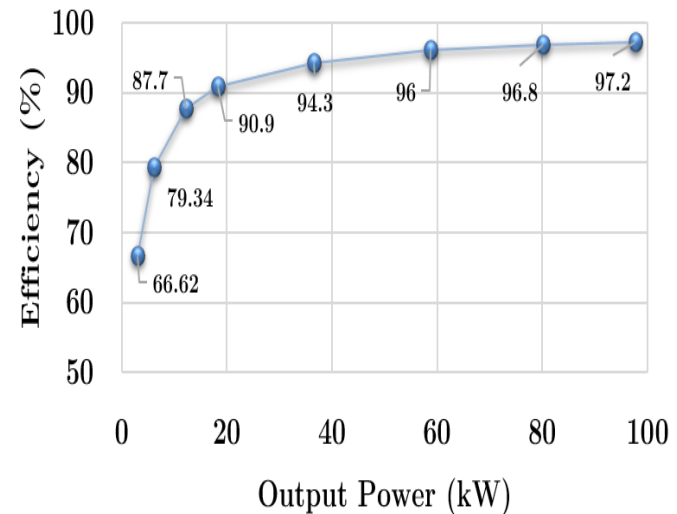
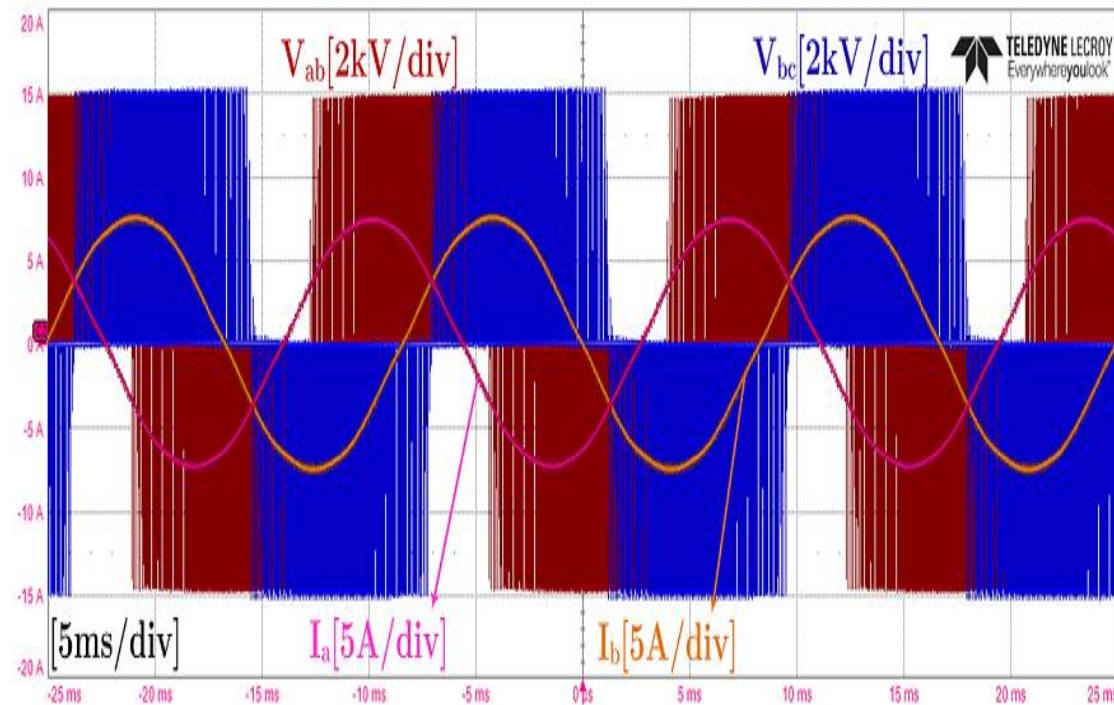
Series connected 3.3kV SiC MOSFET based Three-phase Two-level VSC for MV grid interface

- Series connected 3.3kV SiC MOSFET based Three-phase Two-level VSC has been designed, implemented and tested at MV for direct grid interface



Three-phase Two-level VSC with three series connected 3.3kV SiC MOSFETs per switch
 (a) Inverter circuit used for testing (b) Hardware setup built in the lab

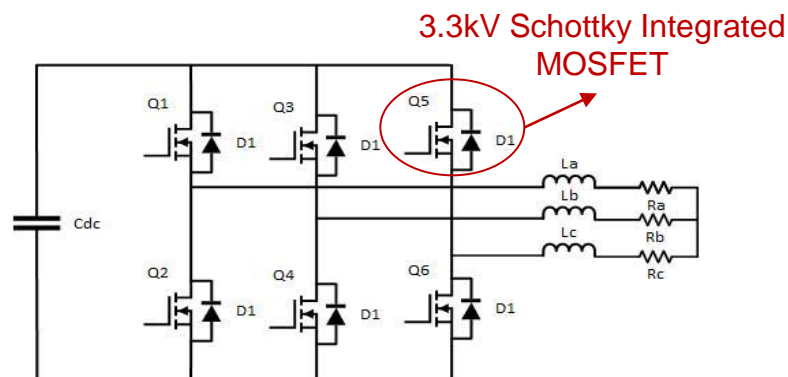
Series connected 3.3kV SiC MOSFET based Three-phase Two-level VSC for MV grid interface



Efficiency vs Power output of the 100 kVA two-level three phase VSC estimated in PLECS simulation by using the switching loss data of the series connected MOSFETs

Experimental results of three-phase VSC in inverter mode of operation at Input dc voltage=6 kV, Input power=19 kW
 Test conditions: Switching frequency= 10kHz, Fundamental frequency=60 Hz, Modulation index=0.6

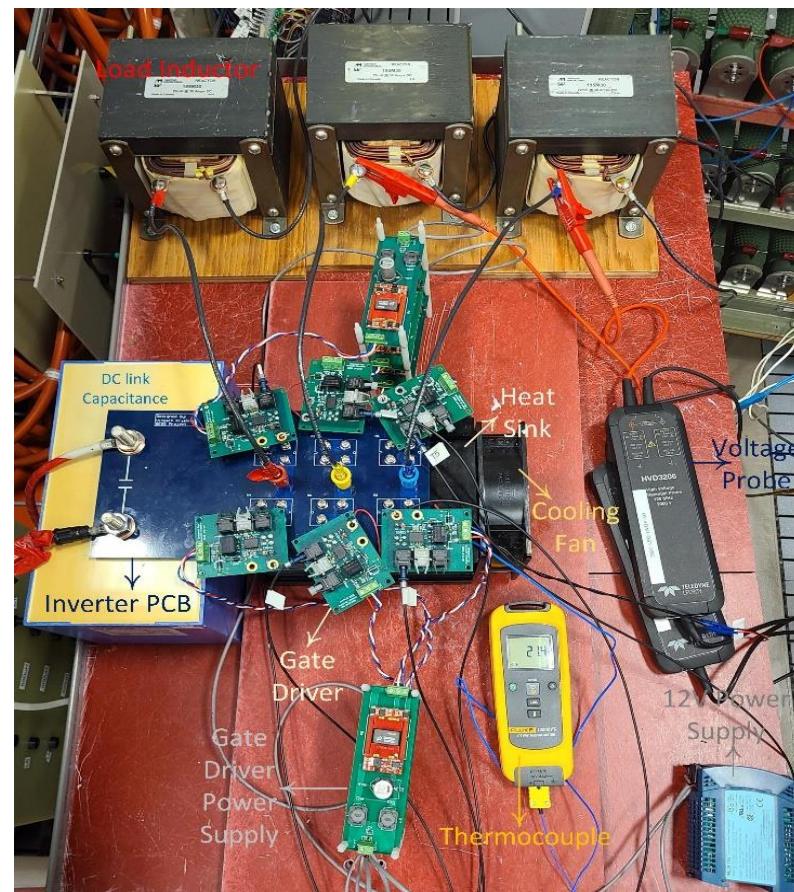
3.3kV Schottky Integrated MOSFET based Three-phase Two-level VSC for MV grid interface



Three-phase Inverter test circuit

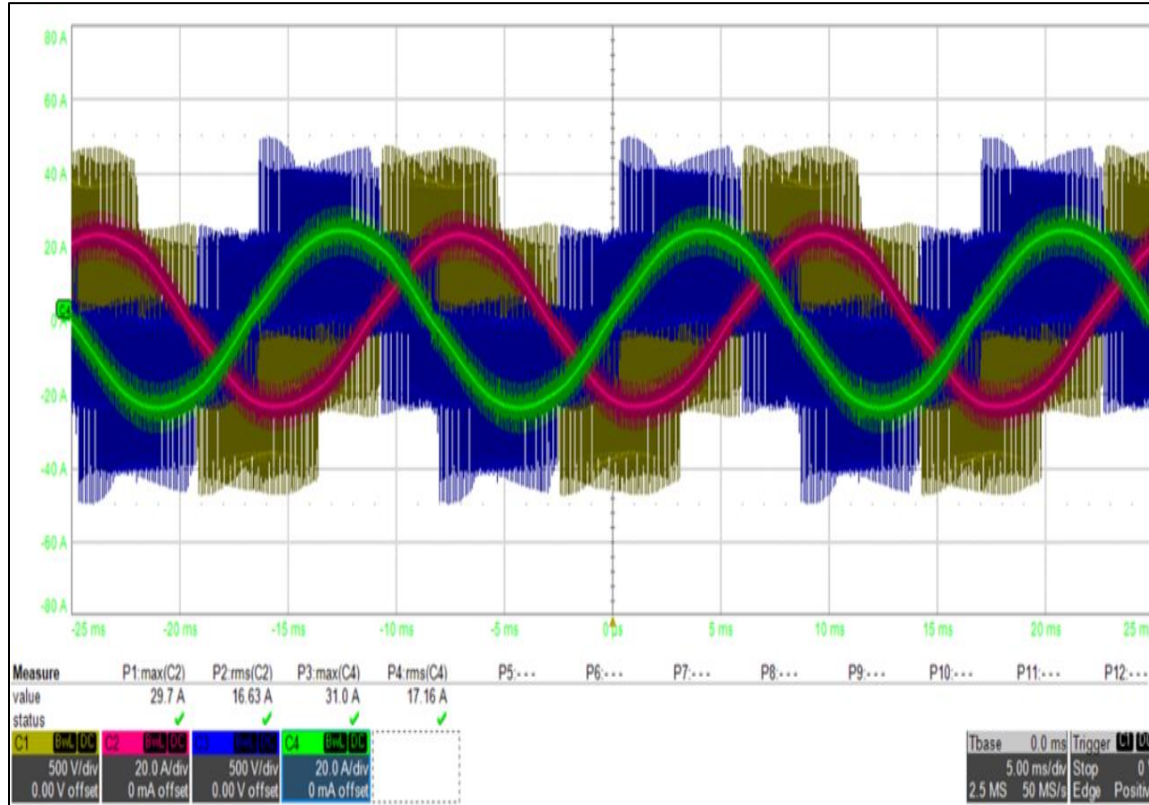
System parameters of the Three-phase Inverter

Parameter	Values
Input Voltage (V_{in})	1500 V
DC link capacitor (C_{dc})	120 μ F
Load Resistance (R_l)	20 Ω
Load Inductance (L_l)	20 mH
Switching frequency (f_{sw})	10 KHz
Line frequency (f_l)	60 Hz
Power factor ($\cos \varphi$)	0.95
Input Power (P_{in})	18.24 kW



Detailed experimental setup of the Three-phase Inverter circuit

3.3kV Schottky Integrated MOSFET based Three-phase Two-level VSC for MV grid interface



Experimental results of the Three-phase Inverter showing Line voltages and phase currents while operating at VDC = 1500 V, m = 0.8



Thermal image of the Inverter during operation

Efficiency Estimation

Equation	Value
$\eta = \frac{P_{in} - P_{loss}}{P_{in}}$	99.01%

Round Trip Efficiency Estimation of MV Grid Connected BESS Power Conditioning System

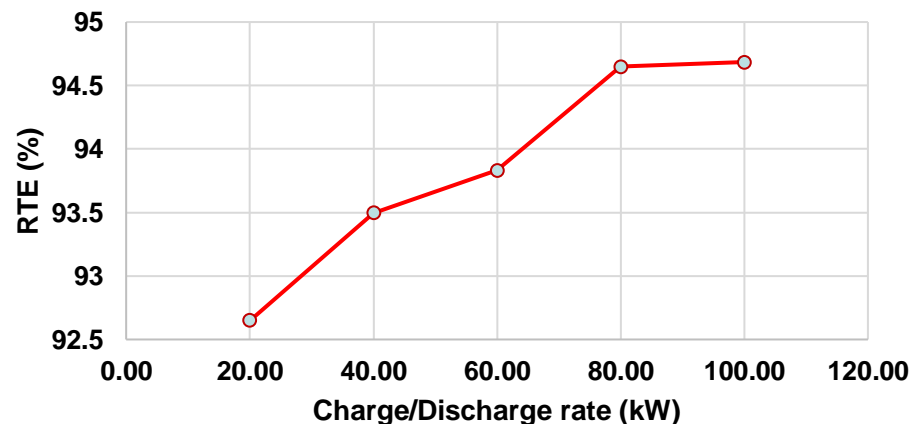
- Round Trip Efficiency (RTE) of the proposed series connected 3.3kV SiC MOSFET based BESS interfacing system is estimated by PLECS simulation

Round Trip Efficiency of the proposed system at nominal operating point of 100kW

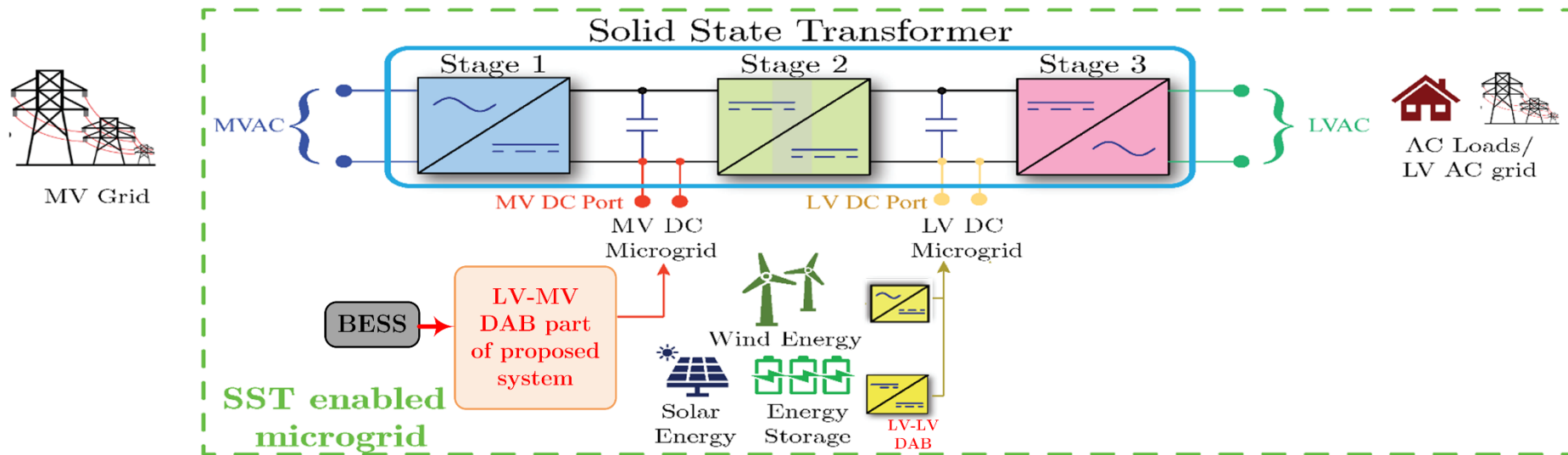
A FEC Efficiency	DAB converter Efficiency	Transformer Efficiency	One way system Efficiency	Round Trip Efficiency
99.53%	98.75%	99%	97.3%	94.68%

Round Trip Efficiency of the proposed system at various charge/discharge rates

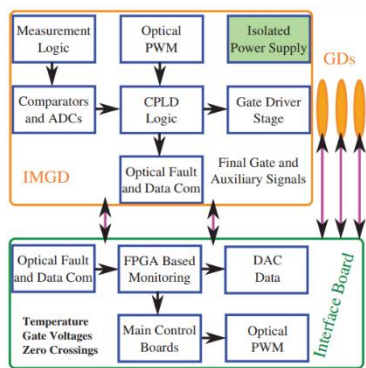
4.16kV Grid - RTE variation with charge/discharge power variation



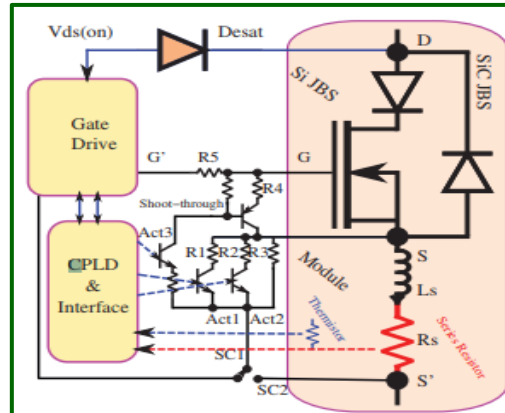
Integration of BESS with SST enables MV DC and AC microgrids



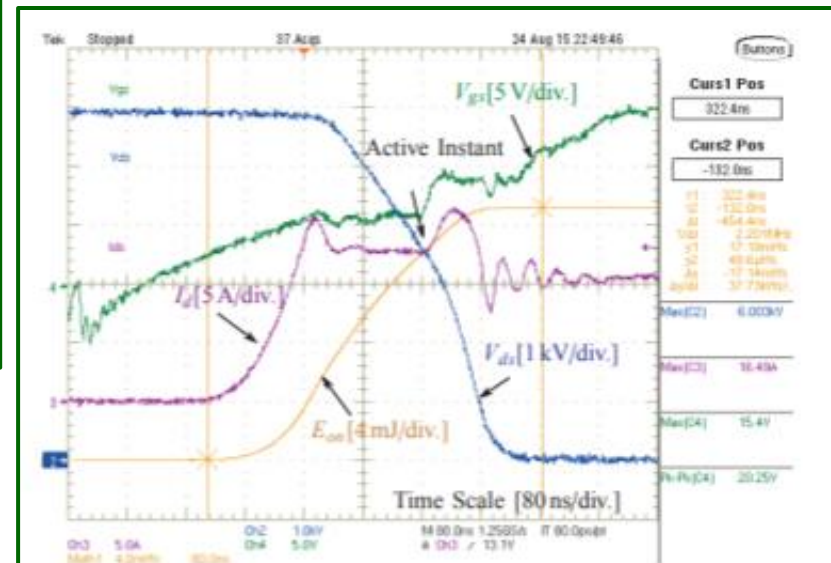
Active Gating and Protection Circuits for SiC Devices with Diagnostics & Prognostics



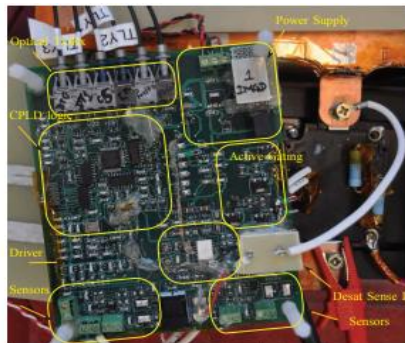
Block Diagram of Intelligent MV Gate Driver



Active gating and protection circuits



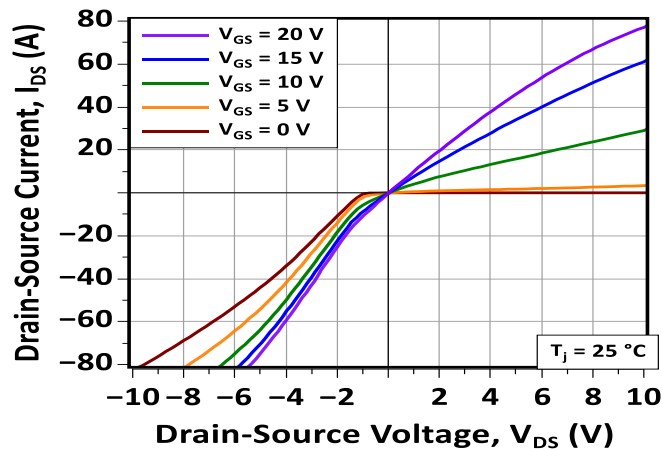
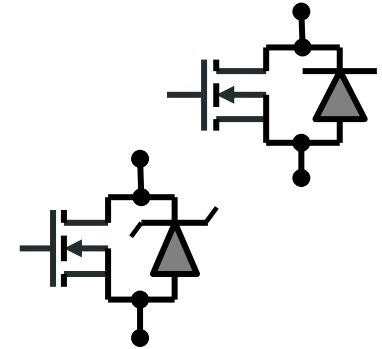
Active gating switching the gate resistance during Turn-on transient to reshape V_{ds}



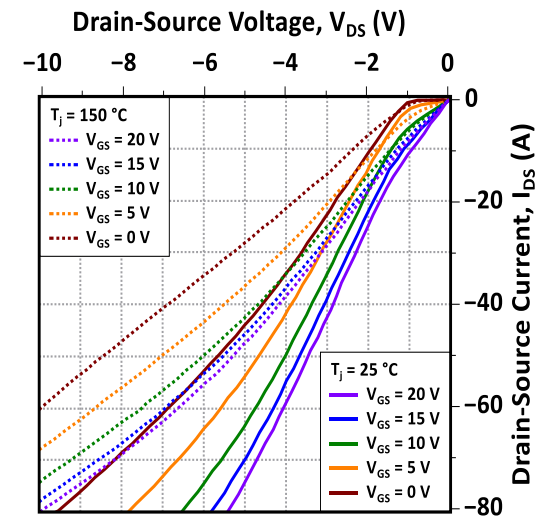
Intelligent Gate Driver Circuit Board

Schottky Integrated SiC MOSFET

- PiN Body diodes are parasitic to standard MOSFET structure. If current flows through this diode, it causes basal-plane dislocations, and often causes MOSFET failure
- Schottky diode prevent bipolar conduction, and hence no Bipolar current



First and Third quadrant I-V characteristics of the 3.3kV Schottky Integrated SiC MOSFET



Third quadrant I-V characteristics - variation with Junction temperature

Schottky Integrated SiC MOSFET: Detailed Characterization

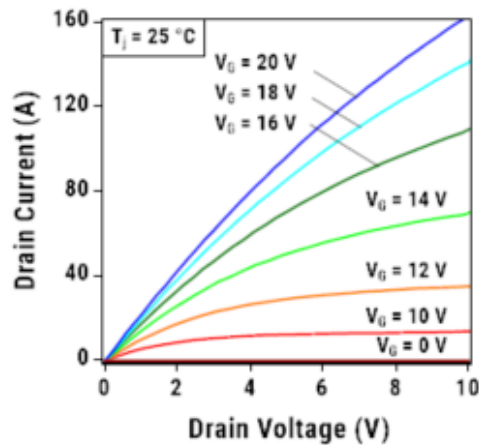


Fig 1. Output Characteristics

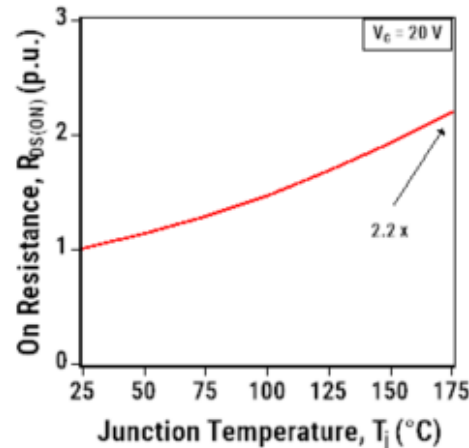


Fig 2. Normalized $R_{DS(ON)}$ vs. Temperature

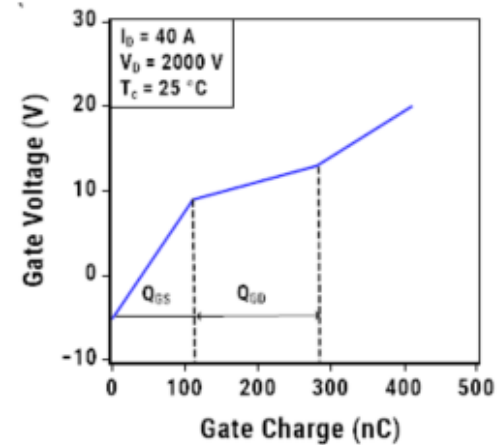


Fig 3. Gate Charge Characteristics

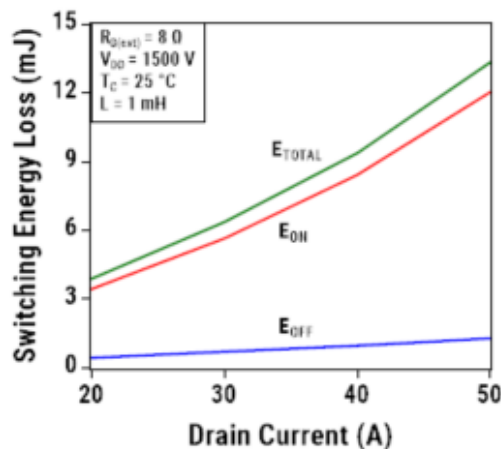


Fig 4. Switching Performance

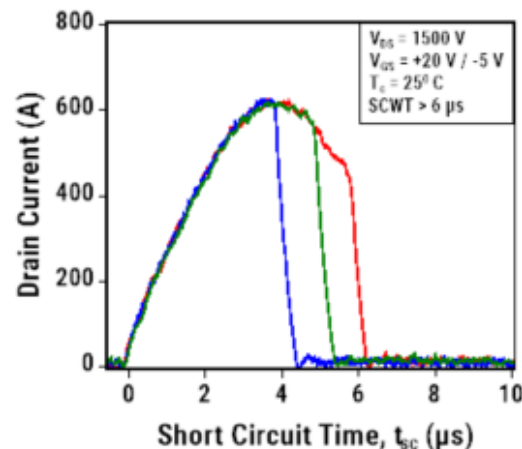


Fig 5. Short Circuit Ruggedness ($> 6\text{ }\mu\text{s}$)

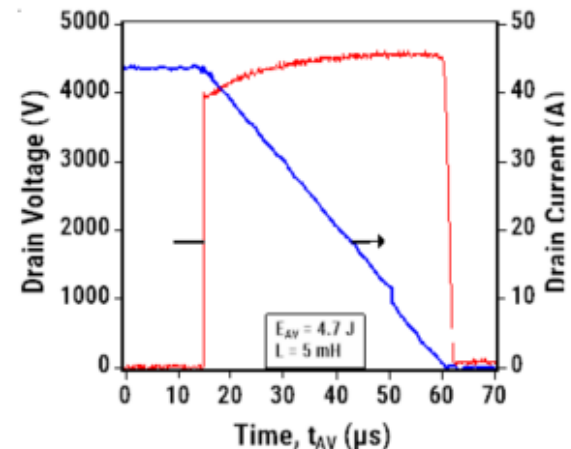


Fig 6. Avalanche Ruggedness (4.7 J)



Conclusions

GeneSiC-NC State Team has demonstrated:

- 3.3kV/50 A MOSFET-diode Integrated Device
- Intelligent Gate Driver with active sensing and control algorithms for stable performance
- BESS Power Conditioning System



Status and Future Efforts

- Current Status
 - Project Started in July 2019 (Phase II on Aug 2020)
 - 3.3kV Monolithically Integrated SiC MOSFET-Schottky Diodes commercialized
 - Gate Driver circuits completed at NCSU/FREEDM
 - Modeling of Circuit Losses being conducted
- Future Efforts (Project end date August 2022)
 - Complete SPICE Modeling of Devices to be used
 - Demonstrate 3.3kV MOSFET-Diodes in BESS
 - Quantify the impact of Monolithic 3.3kV MOSFET-Diode in power electronics on grid-tied energy storage systems



Grant Details

- Principal Investigator: Dr. Ranbir Singh and Prof. Subhashish Bhattacharya
- Program Manager: Dr. Ranbir Singh
- Grantee:
GeneSiC Semiconductor Inc. and North Carolina State University
43670 Trade Center Place
Suite 155
Dulles VA 20166
+1 703 996 8200 (ph)
ranbir.singh@genesicsemi.com